CLAIMS

We claim:

1. A performance monitor for monitoring the occurrence of incidences of one or more events related to the operation of a processor, comprising:

at least one monitor mode control register; and

a plurality of performance monitor counters operatively connected to said monitor mode control register, said monitor mode control register grouping said performance monitor counters so that when one of said performance monitor counters reaches capacity in connection with the counting incidences of a first of said events, a second of said performance monitor counters begins counting subsequent incidences of said first of said events.

2. The performance monitor as set forth in claim 1, wherein the number of occurrences of incidences of events equals X, and the number of performance monitor counters equals Y, whereby said at least one monitor mode control register groups said performance monitor counters into Z groups, wherein $Y \div X = Z$.

3. A performance monitor for monitoring the occurrence of incidences of one or more events related to the operation of a processor, comprising:

at least one control element; and

a plurality of counting elements operatively coupled to said control element, said control element grouping said counting elements so that when one of said counting elements reaches capacity in connection with the counting of incidences of a first of said events, a second of said counting elements begins counting subsequent incidences of said first of said events.

4. The performance monitor as set forth in claim 3, wherein said at least one control element comprises a monitor mode control register.

5. The performance monitor as set forth in claim 4, wherein each of said counting elements comprises a performance monitor counter operatively connected to said monitor mode control register.

6. The performance monitor as set forth in claim 5, wherein the number of occurrences of incidences of events equals X, and the number of performance monitor counters equals Y, whereby said at least one monitor mode control register groups said performance monitor counters into Z groups, wherein $Y \div X = Z$.